In the Claims:

1. (Original) A semiconductor device comprising:

a semiconductor substrate having a recess therein;

a gate insulator on the substrate in the recess;

a gate electrode comprising a first portion on the gate insulator in the recess and a second reduced-width portion extending from the first portion; and

a source/drain region in the substrate adjacent the recess.

2. (Original) The semiconductor device of claim 1, wherein the gate insulator comprises:

a first portion disposed on a sidewall of the recess and having a first thickness; and

a second portion disposed on a bottom of the recess and having a second thickness less than the first thickness.

3. (Original) The semiconductor device of claim 2, wherein the first portion of the gate insulator adjoins a source/drain region in the substrate.

4. (Original) The semiconductor device of claim 2, further comprising a nitride liner disposed between the first portion of the gate insulator and the recessed portion of the gate electrode.

5. (Original) The semiconductor device of Claim 2, further comprising:

an insulation layer on a surface of the substrate adjoining the second portion of the gate electrode above the substrate and extending over a portion of the first portion of the gate electrode; and

an insulating spacer disposed on a sidewall of the second portion of the gate electrode and on the insulation layer.

6. (Original) The semiconductor device of Claim 5, wherein the insulation layer comprises silicon oxide and the insulating spacer comprises silicon nitride.

7. (Original) The semiconductor device of Claim 5, wherein the insulating spacer comprises a first insulating spacer and further comprising a second insulating spacer on sidewalls of the insulation layer and the first insulating spacer.

8. (Original) The semiconductor device of Claim 7, wherein the source/drain region comprises a lighter-doped portion adjoining the recess.

9. (Original) The semiconductor device of Claim 1, wherein the gate electrode further comprises a third portion on the second portion, the third portion having ~~an~~ greater width than the second portion.

10. (Original) The semiconductor device of Claim 9, further comprising:

an insulation layer on a surface of the substrate adjoining the second portion of the gate electrode above the substrate and extending over a portion of the first portion of the gate electrode; and

an insulating spacer disposed on a sidewall of the second portion of the gate electrode, on a sidewall of the third portion of the gate electrode and on the insulation layer.

11. (Original) The semiconductor device of Claim 10, wherein the insulation layer comprises silicon oxide and the insulating spacer comprises silicon nitride.

12. (Original) The semiconductor device of Claim 9, wherein the gate insulator comprises:

a first portion disposed on a sidewall of the recess and having a first thickness; and

a second portion disposed on a bottom of the recess and having a second thickness less than the first thickness.

13. (Original) The semiconductor device of Claim 12, wherein the source/drain region comprises a lighter-doped portion adjoining the first portion of the gate insulator.

14. (Original) The semiconductor device of Claim 9, wherein the gate insulator comprises a substantially uniform thickness insulation layer lining the recess.

15. (Original) The semiconductor device of Claim 1, wherein the source/drain region comprises a lighter-doped portion nearer the recess.

16. (Original) The semiconductor device of Claim 1, wherein the recess has a curved shape.

17. (Original) The semiconductor device of Claim 16, wherein the recess is hemispherical or elliptical.

18.-39. (Cancelled).